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### Features

- Highly Optimized drop-in module for Virtex™, Virtex-E™ and Spartan II™ FPGAs
- Ultra High performance 16 point complex FFT
- 16 bit input and output data
- Fits in XCV100 - fixed scale core fits in a 20h x 25w CLB rectangle
- Natural order input and output
- Sample per clock streaming input and output
- Synchronize input allows variable spacing between input data sets
- No Block RAMs used
- Relatively Placed Macro (RPM) guarantees performance and density
- Use with v3.1i or later Xilinx Coregen system
- Relatively Placed Macro guarantees density and performance
- Fixed and Dynamic scale versions included

### Applications

The FFT core is used to transform a time domain sequence to a frequency domain representation of the data. Inverse Fourier Transforms may be obtained by conjugating the input and output of the FFT. When combined with reordering memory and a phase rotator, this 16 point kernel can be used as a building block for larger transforms.

### General Description

The FFT core set uses the Winograd 16 point Fast Fourier Transform algorithm to compute the 16 point discrete Fourier transform of a complex vector. The core accepts 16 bit data on the real and imaginary inputs and outputs 16 bit data on each of the real and imaginary outputs.

Core Facts	
Core Specifics	
Device Families	Virtex, VirtexE, VirtexEM, SpartanII
CLBs Used	Fixed 973 slices in a scale: 25 W x 20 H area
	Dynamic TBD slices in a scale: 27 W x 20 H area
IOBs Used	none in macro (33 inputs, 33 outputs plus clock, + 3 extra inputs for dynamic scale)
System clock	System clock: >133 MHz
Clock Latency	73 clocks (76 for dynamic scaling)
Device Features used	Carry logic, CLB Shift registers, relative placement

Supported Devices	
Family and speed grade	Maximum clock for speed grade
Virtex-4	140 MHz
VirtexE-8	240 MHz
Minimum device size	XCV100 / XC2S100

Provided with Core Set	
Cores Included	<ul style="list-style-type: none"> <li>• Fixed scale by 1, 1/2, 1/4, 1/8, and 1/16, FFT cores.</li> <li>• Dynamic scale FFT core.</li> <li>• 2's complement core (to make core into IFFT)</li> </ul>
Documentation	Core interface document
Design file format	EDIF netlists VHDL source available at extra cost
Constraints	.UCF file with timing constraint. Placement information is embedded in design
Entry/ Verification tools	VHDL – Synplicity Simulate using Aldec or Modelsim
Schematic symbols	Viewlogic
Evaluation model	Compiled Modelsim or Aldec design, Matlab model
Reference Designs and application notes	Placed macros for conjugating for IFFT
Additional Items	none

Design tools	
Xilinx Core tools	M3.1i sp5
Design verification	Aldec or Modelsim simulators

Support	
Provided by Andraka Consulting Group	

## Ultra-Fast 16 point complex FFT

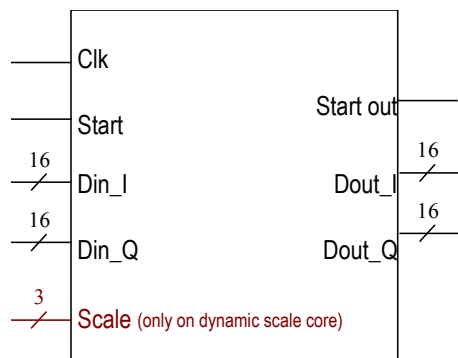


Figure 1. 16 Point FFT symbol

Table 1. FFT interface signals

Signal	Direction	Description
CLK	Input	System clock. Active on rising edge
START	Input	'1' marks first sample of FFT to synchronize internal timing to data. Does not affect complete data sets already in FFT pipeline
DIN_I[15:0]	Input	Input Data bus, real (In-phase) component. Bit 15 is most significant bit. Accepted on rising edge of CLK.
DIN_Q[15:0]	Input	Input Data bus, imaginary (Quadrature) component. Bit 15 is most significant bit. Accepted on rising edge of CLK.
SCALE [2:0] (Dynamic Scale Core only)	Input	Sets scaling of CORE. Value determines number of bits result is right shifted. Valid for 0 (000) to 4 (100).
START_OUT	Output	Delayed copy of START input. '1' indicates first sample of output
Dout_I[15:0]	Output	Output Data bus, real (In-phase) component. Bit 15 is most significant bit. Updated on rising edge of CLK.
Dout_Q[15:0]	Output	Output Data bus, imaginary (Quadrature) component. Bit 15 is most significant bit. Updated on rising edge of CLK.

## Core Modifications

The core is provided as a black box relatively placed macro (RPM). Andraka Consulting Group, Inc can customize or retarget the core for additional cost. This includes changing input and output precision, scaling or alternate layouts. The design source (VHDL for Synplicity) is available at additional cost.

### Pinout

Signal names for interfacing the core are shown in figure 1 and described in table 1. Inputs have a fan-in of 2 loads, outputs are registered.

### Verification Methods

The FPGA core was verified through functional simulation and static timing analysis. Functional simulation included comparison of the logic outputs with Matlab simulations. Timing information is obtained using the static timing analysis in the Xilinx tools.

### Ordering Information

This product is available directly from Andraka Consulting Group, Inc. Please contact them for further information and pricing.

### Recommended Design Experience

Users should be familiar with standard Xilinx tool flows and using black box cores. The designer should also be familiar with high performance FPGA design and floorplanning in order to design surrounding circuits capable of matching the performance of this core.

### Related Information

S. Winograd, "On Computing the Discrete Fourier Transform," *Mathematics of Computation*, Vol. 32, No. 141, pp. 175-199 (1978).

R. E. Blahut, *Fast Algorithms for Digital Signal Processing*, Addison Wesley Longman, Inc, 1985

W. W. Smith and J. M. Smith, *Handbook of Real-Time Fast Fourier Transforms*, IEEE press, New York, 1995.

L. R. Rabiner and B. Gold, *Theory and Application of Digital Signal Processing*, Prentice-Hall Inc, Englewood Cliffs, New Jersey, 1975.

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